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**DIVISION 2, G4**

**DECO LAB**

**ASSIGNMENT 9**

**Aim:** Flip flops (JK, D, T).

**Q 1 : Write a Verilog code to implement J-K flip flop and validate the code via a suitable Test bench code.**

* **Design Code:**

module jkff(input reset, input clk, input j, input k, output reg q, output qnot);

assign qnot=~q;

always @(posedge clk)

if (reset) q<=1'b0; else

case ({j, k})

2'b00: q<=q;

2'b01: q<=1'b0;

2'b10: q<=1'b1;

2'b11: q<=~q;

endcase

endmodule

* **Testbench Code:**

module test;

reg clk=0;

reg j=0;

reg k=0;

reg reset=1;

wire q, qnot;

jkff dut(reset, clk,j,k,q,qnot);

initial

begin

$dumpfile("dump.vcd");

$dumpvars(1);

j=1'b1;

k=1'b1;

#5 reset=1'b0;

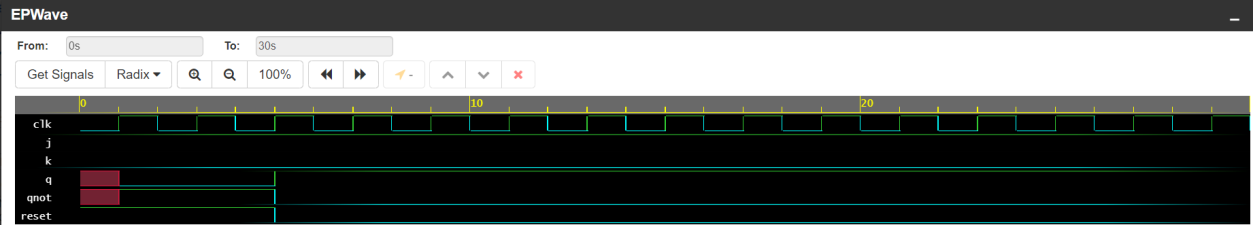
#25 $finish;

end

always #1 clk=~clk;

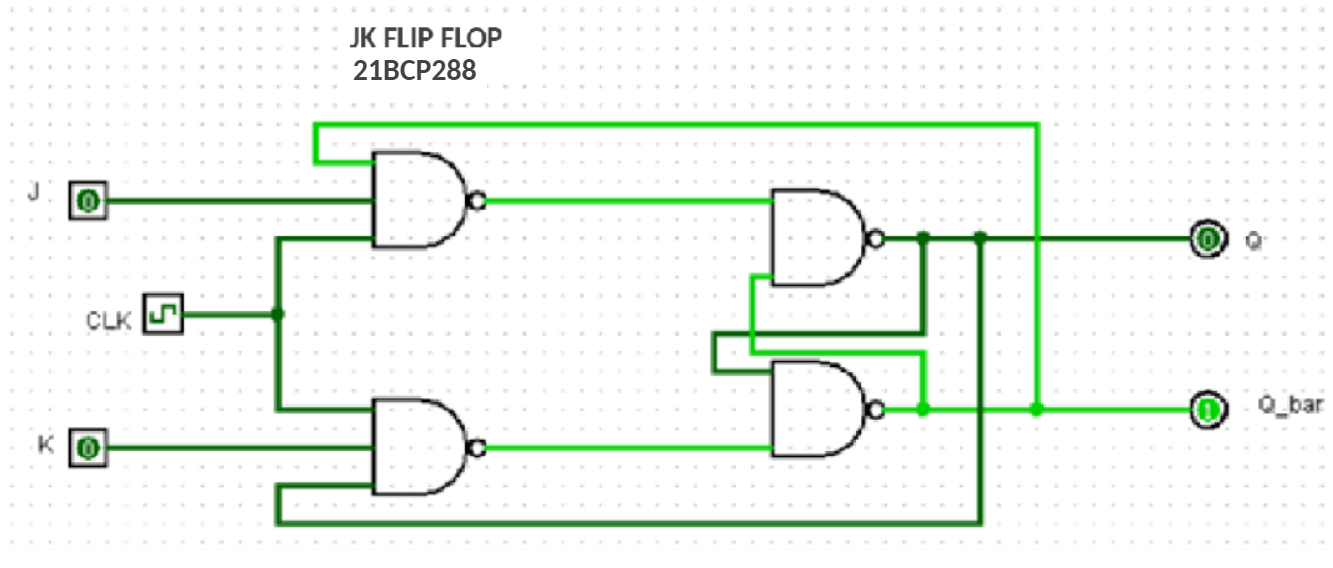
endmodule

* **Waveform:**

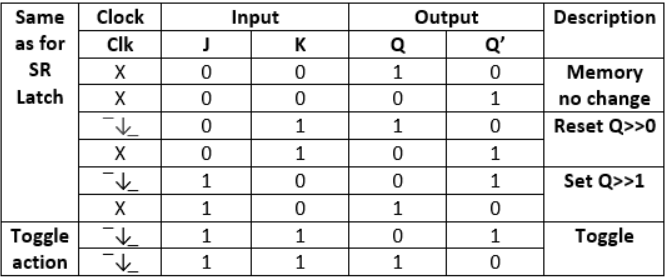


**Q 2 : Design a J-K flip flop in Logisim and validate the circuit.**

* **Circuit:**



* **Truth Table:**

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**Q 3 : Write a Verilog code to implement D flip flop and validate the code via a suitable Test bench code.**

* **Design Code:**

module dff(input reset, input clk, input d, output reg q, output qnot);

assign qnot=~q;

always @(posedge clk)

if (reset) q<=1'b0; else

case ({d})

2'b0: q<=1'b0;

2'b1: q<=1'b1;

endcase

endmodule

* **Testbench Code:**

module test;

reg clk=0;

reg d=0;

reg reset=1;

wire q, qnot;

dff dut(reset, clk, d, q,qnot);

initial

begin

$dumpfile("dump.vcd");

$dumpvars(1);

d=1'b0;

#5 reset=1'b0;

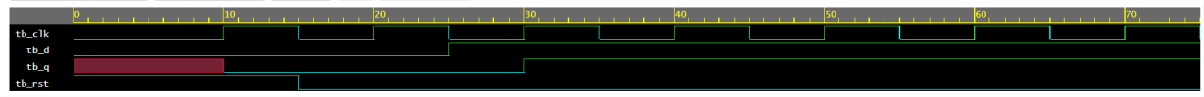
#25 $finish;

end

always #1 clk=~clk;

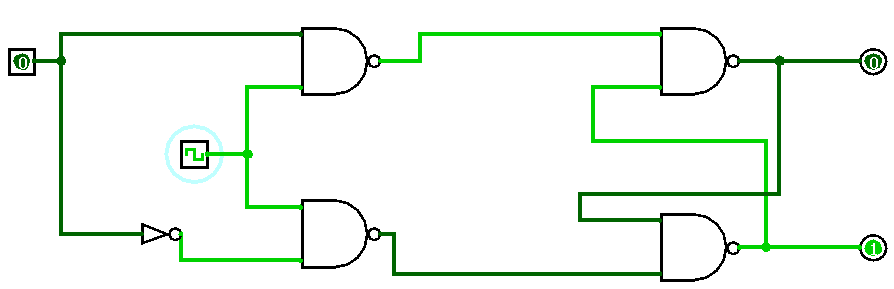
endmodule

* **Waveform:**

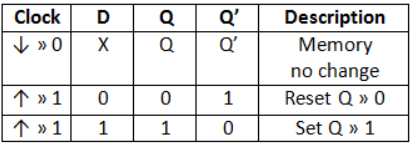


**Q 4 : Design a D flip flop in Logisim and validate the circuit.**

* **Circuit:**

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* **Truth Table:**

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**Q 5 : Write a Verilog code to implement T flip flop and validate the code via a suitable Test bench code.**

* **Design Code:**

module tff(input reset, input clk, input t, output reg q, output qnot);

assign qnot=~q;

always @(posedge clk)

if (reset) q<=1'b0; else

case ({t})

1'b0: q<=q;

1'b1: q<=~q;

endcase

endmodule

* **Testbench Code:**

module test;

reg clk=0;

reg t=0;

reg reset=1;

wire q, qnot;

tff dut(reset, clk, t, q, qnot);

initial

begin

$dumpfile("dump.vcd");

$dumpvars(1);

t=1'b0;

#5 reset=1'b0;

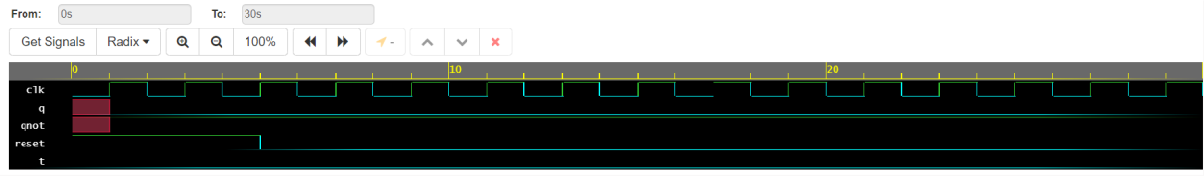
#25 $finish;

end

always #1 clk=~clk;

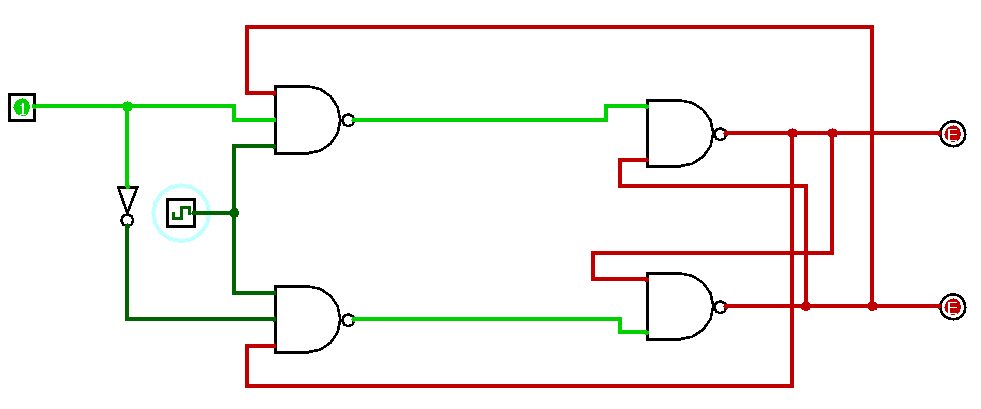
endmodule

* **Waveform:**

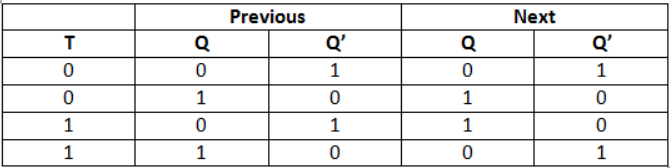


**Q 6 : Design a T flip flop in Logisim and validate the circuit.**

* **Circuit:**

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* **Truth Table:**

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